

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:
 - a semiconductor layer;
 - a source region provided in the semiconductor layer;
 - 5 a drain region provided in the semiconductor layer so as to be spaced apart from the source region;
 - a gate insulating film provided on the semiconductor layer;
 - a gate electrode provided on the gate insulating film;
 - a first interlevel insulating film provided on the semiconductor layer so as to cover 10 the gate electrode;
 - a first gate interconnect provided on the first interlevel insulating film so as to be electrically connected to the gate electrode;
 - a first drain interconnect provided on the first interlevel insulating film so as to be electrically connected to the drain region; and
- 15 a second interlevel insulating film formed on the first interlevel insulating film so as to cover the first gate interconnect and the first drain interconnect, wherein part of the first gate interconnect extends in the gate width direction so that the parts of the first drain interconnect and part of the first gate interconnect face each other with part of the second interlevel insulating film interposed therebetween.

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2. The semiconductor device of claim 1, further comprising a second drain interconnect provided on the second interlevel insulating film so as to be electrically connected to the first drain interconnect.

25 3. The semiconductor device of claim 2, wherein the thicknesses of the first drain

interconnect and the first gate interconnect are larger than that of the second drain interconnect.

4. The semiconductor device of claim 1, wherein the part of the second interlevel insulating film interposed between the parts of the first drain interconnect and the first gate interconnect is formed of a high dielectric material.

5. The semiconductor device of claim 4, wherein the high dielectric material is silicon nitride.

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6. The semiconductor device of claim 2, further comprising:
a second gate interconnect provided on the second interlevel insulating film so as to be electrically connected to the first gate interconnect; and
a third interlevel insulating film provided on the second interlevel insulating film so as to cover the second drain interconnect and the second gate interconnect,
wherein parts of the second drain interconnect and the second gate interconnect extend so as to face each other.

20 7. The semiconductor device of claim 6, wherein part of the third interlevel insulating film interposed between the parts of the second drain interconnect and the second gate interconnect is formed of a high dielectric material.

8. The semiconductor device of claim 7, wherein the high dielectric material is silicon nitride.

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9. The semiconductor device of claim 1, further comprising a first source interconnect provided on the first interlevel insulating film so as to be electrically connected to the source region,

wherein the distance between the first source interconnect and the first gate interconnect is larger than that between the first drain interconnect and the first gate interconnect.

10. The semiconductor device of claim 1, wherein the drain region is electrically connected to an internal circuit and an input/output terminal that can input a signal into the internal circuit.

11. The semiconductor device of claim 1, wherein the gate electrode is electrically connected to a resistance.

15 12. A method for fabricating a semiconductor device, comprising:
the step a) of forming a gate electrode on a semiconductor layer with a gate insulating film interposed therebetween;

the step b) of forming source and drain regions in the semiconductor layer;

the step c) of forming a first interlevel insulating film over the semiconductor layer

20 after the step b);

the step d) of forming a first gate interconnect on the first interlevel insulating film so as to be electrically connected to the gate electrode and extend in the gate width direction;

the step e) of forming a first drain interconnect on the first interlevel insulating film

25 so as to be electrically connected to the drain region and have part facing part of the first

gate interconnect in the gate width direction; and

the step f) of forming a second interlevel insulating film on the first interlevel insulating film so as to cover the first gate interconnect and the first drain interconnect.

5 13. The method of claim 12, further comprising the step g) of forming a second drain interconnect on the second interlevel insulating film so as to be electrically connected to the first drain interconnect.

10 14. The method of claim 13, wherein the thicknesses of the first drain interconnect and the first gate interconnect are larger than that of the second drain interconnect.

15 15. The method of claim 13, further comprising the step h) of forming a second gate interconnect on the second interlevel insulating film so as to be electrically connected to the first gate interconnect and have part facing part of the second drain interconnect.

15 16. The method of claim 15, further comprising, after the step h), the step j) of forming a third interlevel insulating film in which at least part is formed of a high dielectric material on the second interlevel insulating film.

20 17. The method of claim 11, wherein in the step f), part of the second interlevel insulating film is formed of a high dielectric material.

25 18. The method of claim 11, further comprising the step i) of forming a first source interconnect on the first interlevel insulating film so as to be electrically connected to the source region,

wherein the distance between the first source interconnect and the first gate interconnect is larger than that between the first drain interconnect and the first gate interconnect.